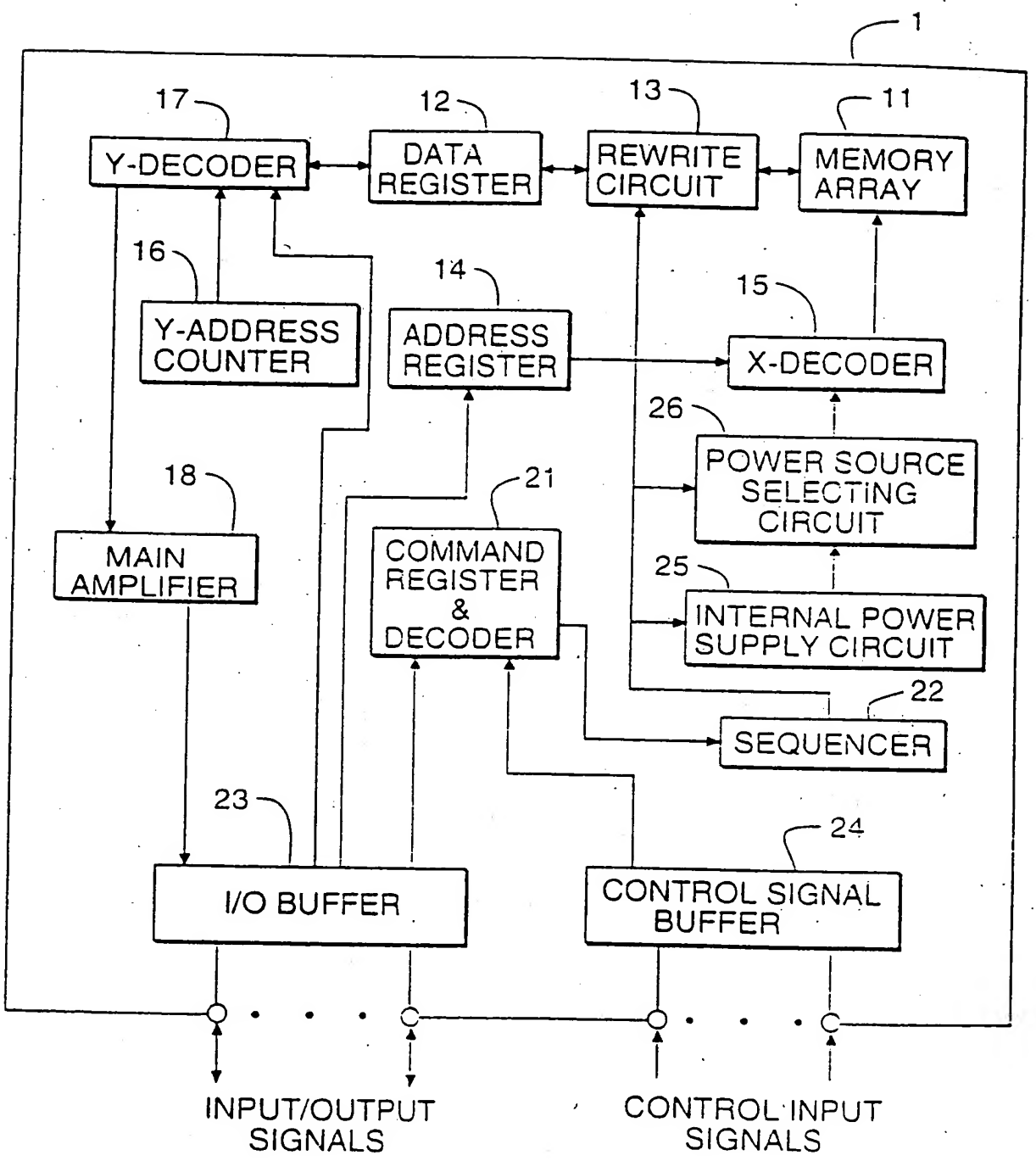

1
17
Y-DECODER
12
DATA REGISTER
13
REWRITE CIRCUIT
11
MEMORY ARRAY
16
Y-ADDRESS COUNTER
14
ADDRESS REGISTER
15
X-DECODER
26
POWER SOURCE SELECTING CIRCUIT
18
MAIN AMPLIFIER
21
COMMAND REGISTER & DECODER
25
INTERNAL POWER SUPPLY CIRCUIT
22
SEQUENCER
23
I/O BUFFER
24
CONTROL SIGNAL BUFFER
INPUT/OUTPUT SIGNALS
CONTROL INPUT SIGNALS

FIG. 1

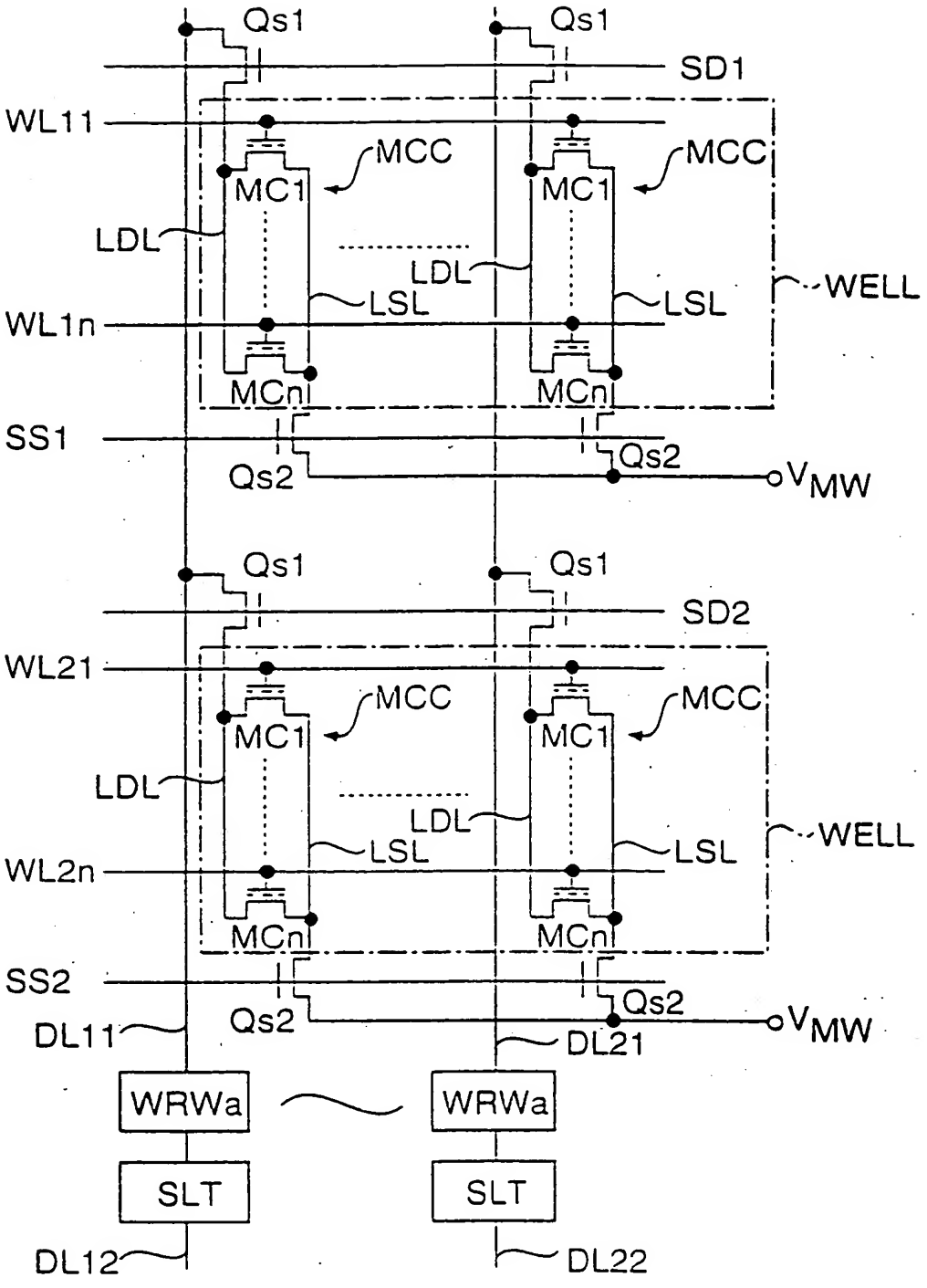

Qs1
Qs1
SD1
WL11
MCC
MCC
MC1
MC1
LDL
LDL
WELL
LSL
LSL
WL1n
MCn
MCn
SS1
Qs2
Qs2
V_{MW}
Qs1
Qs1
SD2
WL21
MCC
MCC
MC1
MC1
LDL
LDL
WELL
LSL
LSL
WL2n
MCn
MCn
SS2
Qs2
Qs2
V_{MW}
DL11
DL21
WRWa
WRWa
SLT
SLT
DL12
DL22

FIG. 2

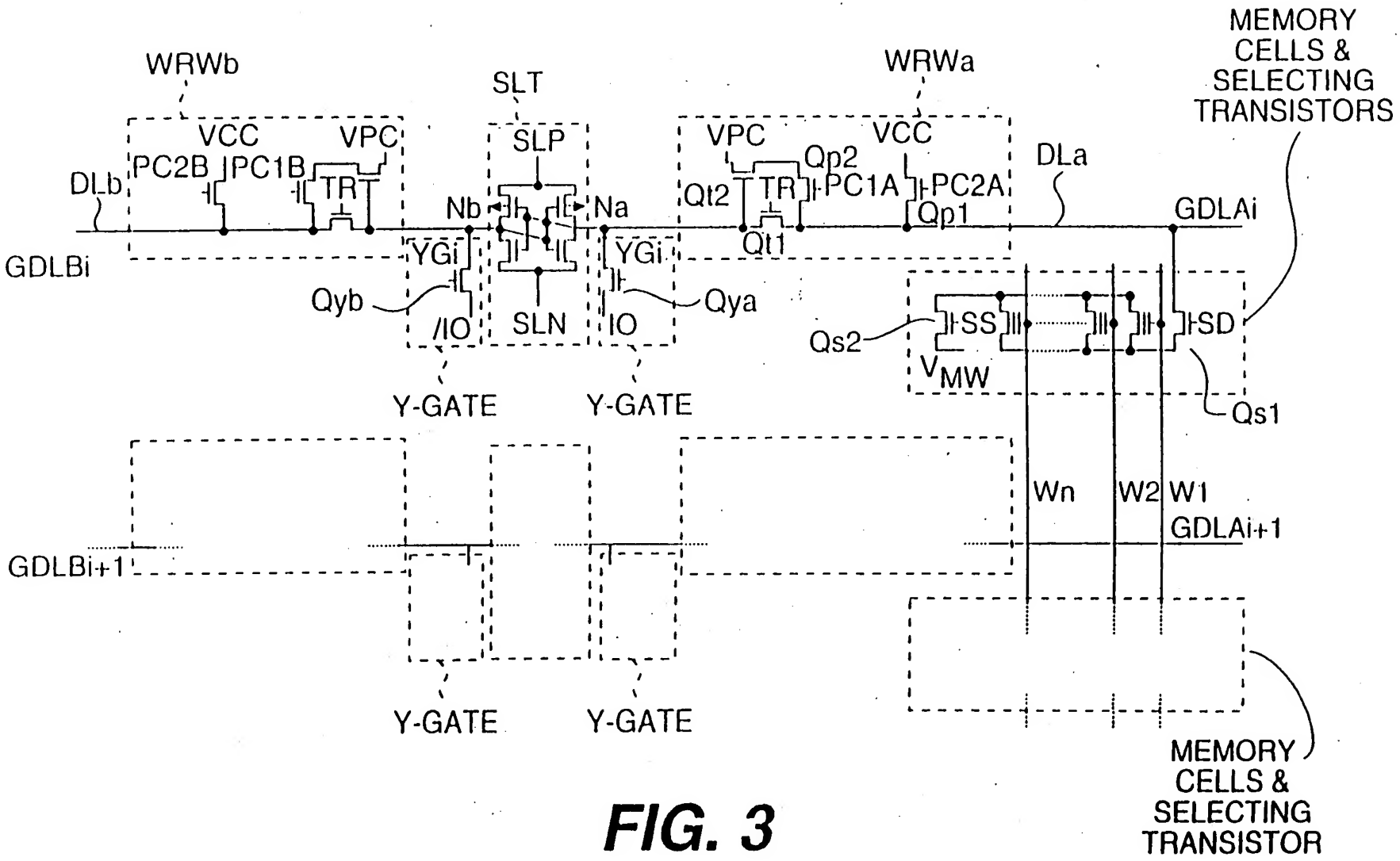

WRWb
SLT
WRWa
MEMORY CELLS & SELECTING TRANSISTORS
VCC
PC2B
PC1B
VPC
TR
SLP
VPC
Qp2
VCC
DLa
DLb
Nb
Na
Qt2
TR
PC1A
PC2A
Qp1
GDLAi
GDLBi
YGi
YGi
Qt1
Qyb
Qya
/IO
SLN
IO
Qs2
SS
SD
V_{MW}
Qs1
Y-GATE
Y-GATE
Wn
W2
W1
GDLAi+1
GDLBi+1
Y-GATE
Y-GATE
MEMORY CELLS & SELECTING TRANSISTOR

FIG. 3

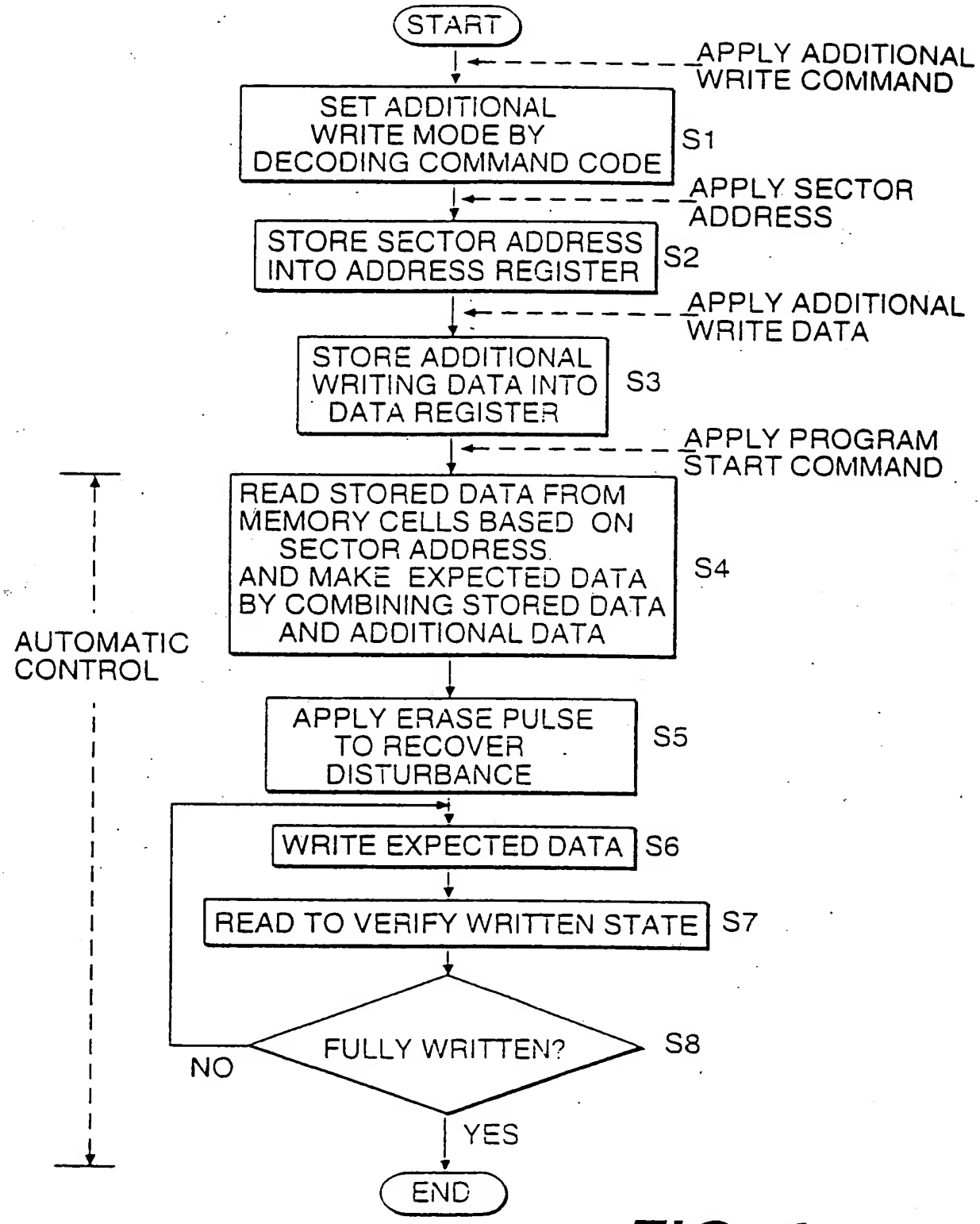

START
APPLY ADDITIONAL WRITE COMMAND
SET ADDITIONAL WRITE MODE BY DECODING COMMAND CODE
S1
APPLY SECTOR ADDRESS
STORE SECTOR ADDRESS INTO ADDRESS REGISTER
S2
APPLY ADDITIONAL WRITE DATA
STORE ADDITIONAL WRITING DATA INTO DATA REGISTER
S3
APPLY PROGRAM START COMMAND
READ STORED DATA FROM MEMORY CELLS BASED ON SECTOR ADDRESS AND MAKE EXPECTED DATA BY COMBINING STORED DATA AND ADDITIONAL DATA
S4
AUTOMATIC CONTROL
APPLY ERASE PULSE TO RECOVER DISTURBANCE
S5
WRITE EXPECTED DATA
S6
READ TO VERIFY WRITTEN STATE
S7
FULLY WRITTEN?
S8
NO
YES
END

FIG. 4

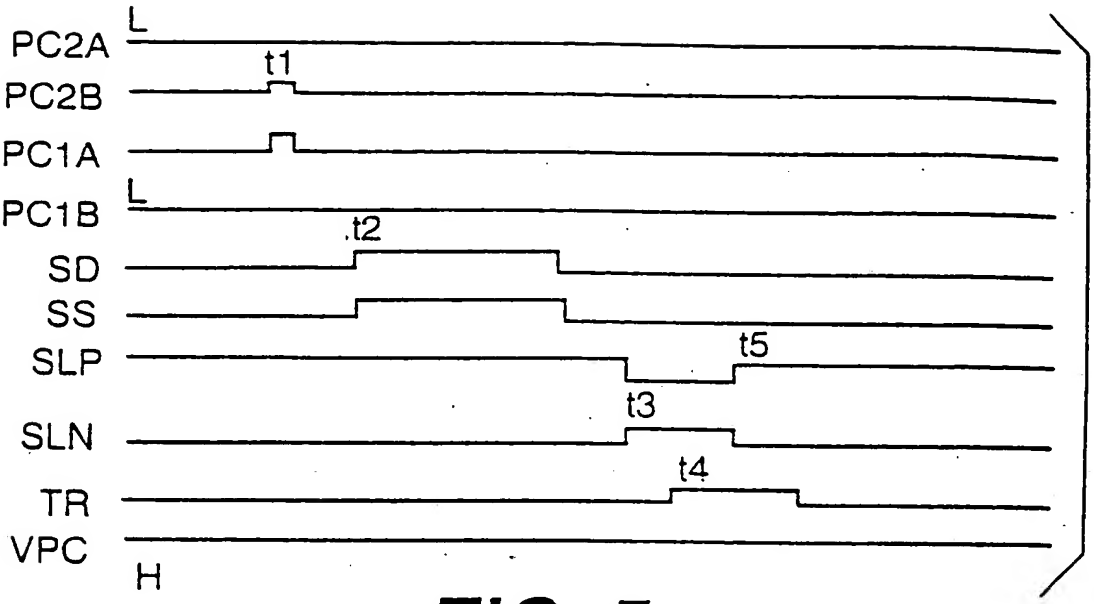


FIG. 5

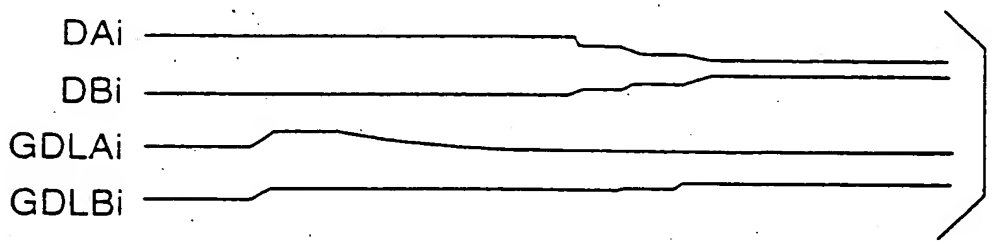


FIG. 6(a)

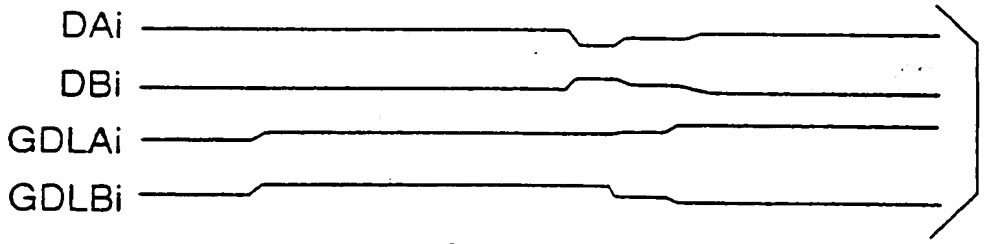


FIG. 6(b)

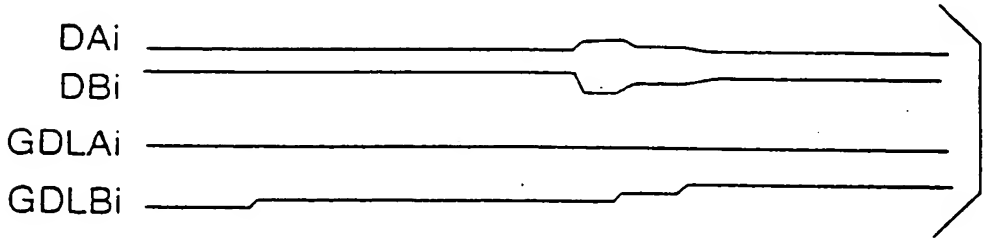


FIG. 6(c)

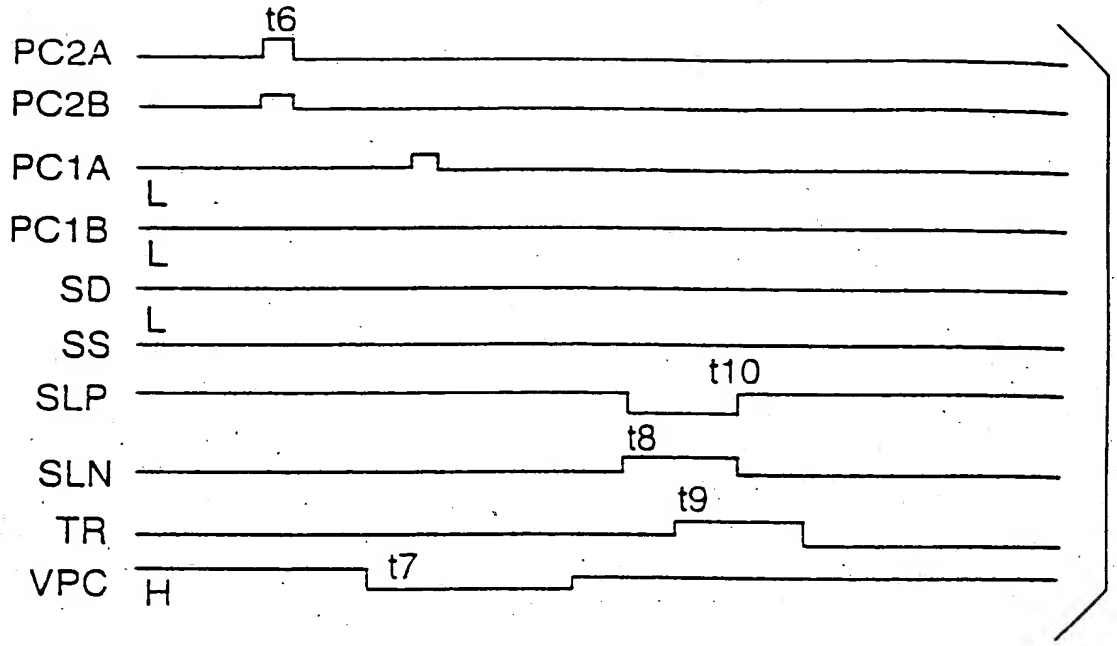


FIG. 7

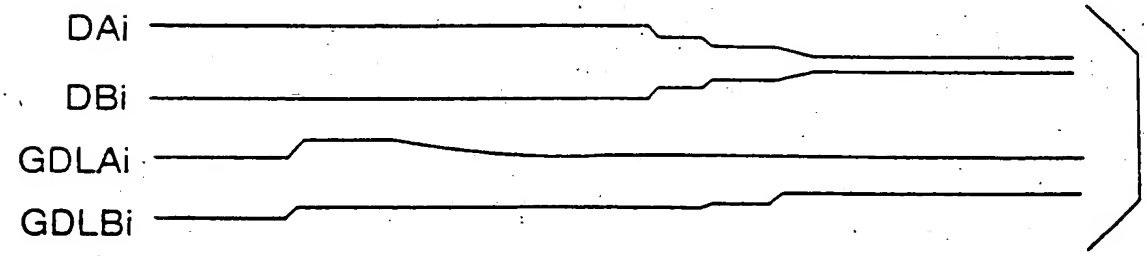


FIG. 8(a)

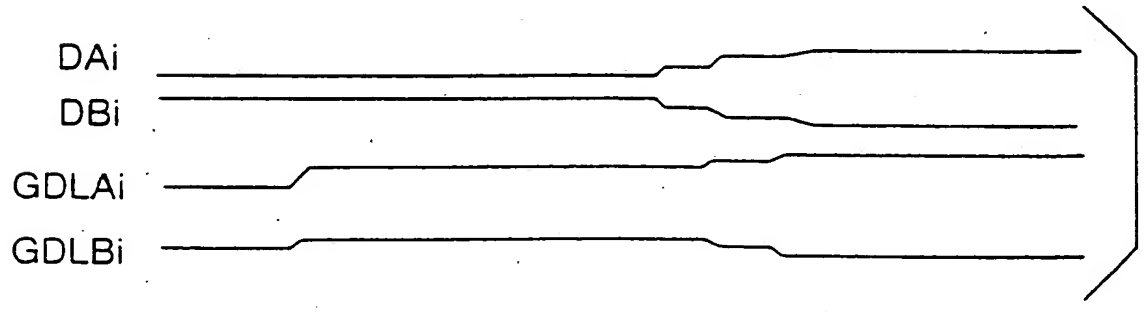


FIG. 8(b)

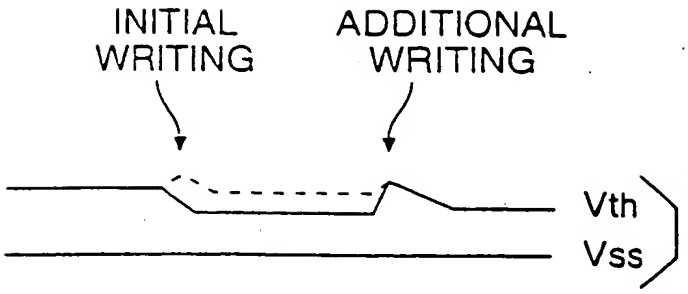


FIG. 9(a)

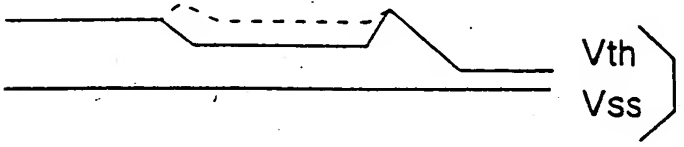


FIG. 9(b)

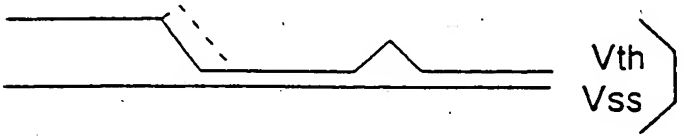


FIG. 9(c)

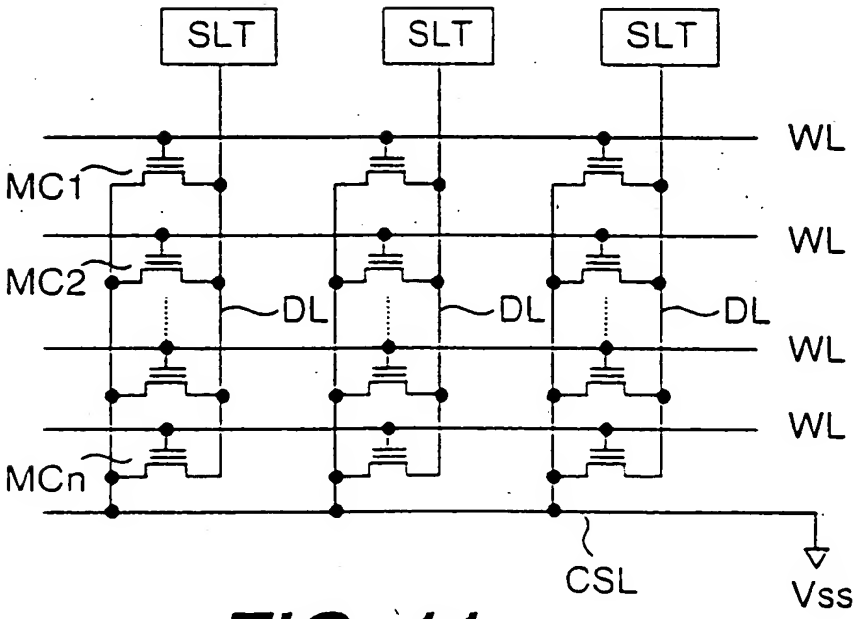


FIG. 11

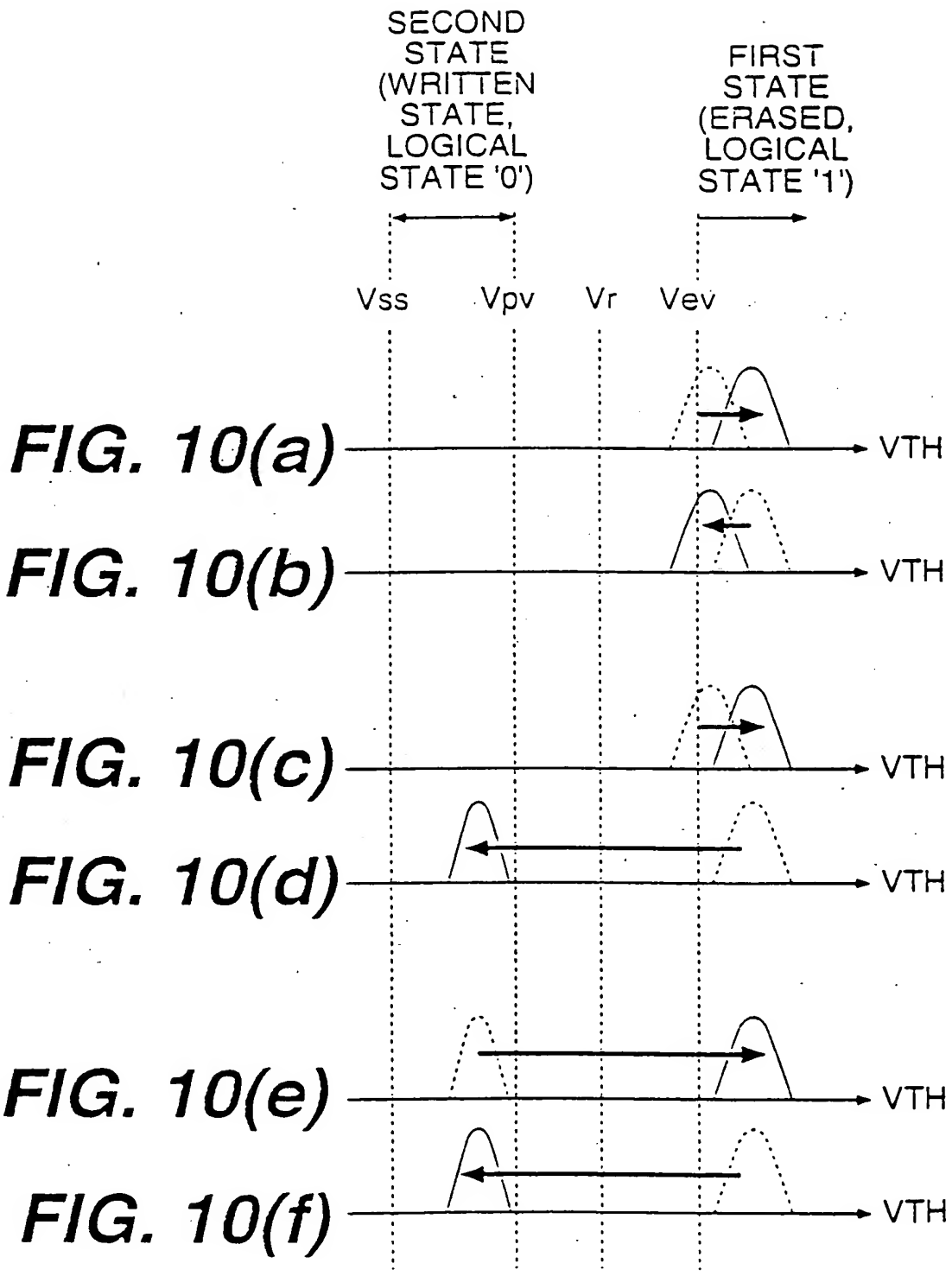


FIG. 10(a)

FIG. 10(b)

FIG. 10(c)

FIG. 10(d)

FIG. 10(e)

FIG. 10(f)

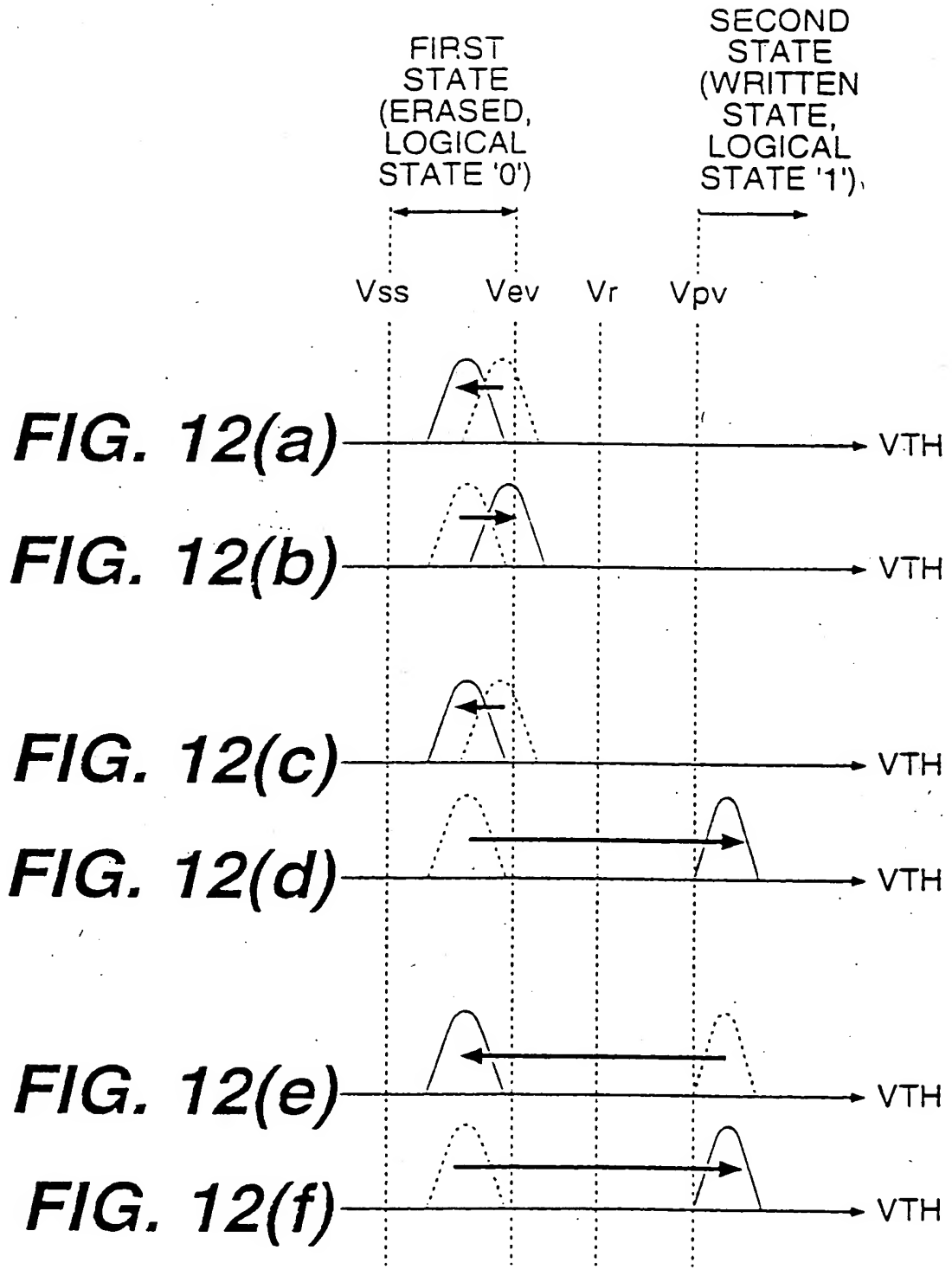


FIG. 12(a)

FIG. 12(b)

FIG. 12(c)

FIG. 12(d)

FIG. 12(e)

FIG. 12(f)

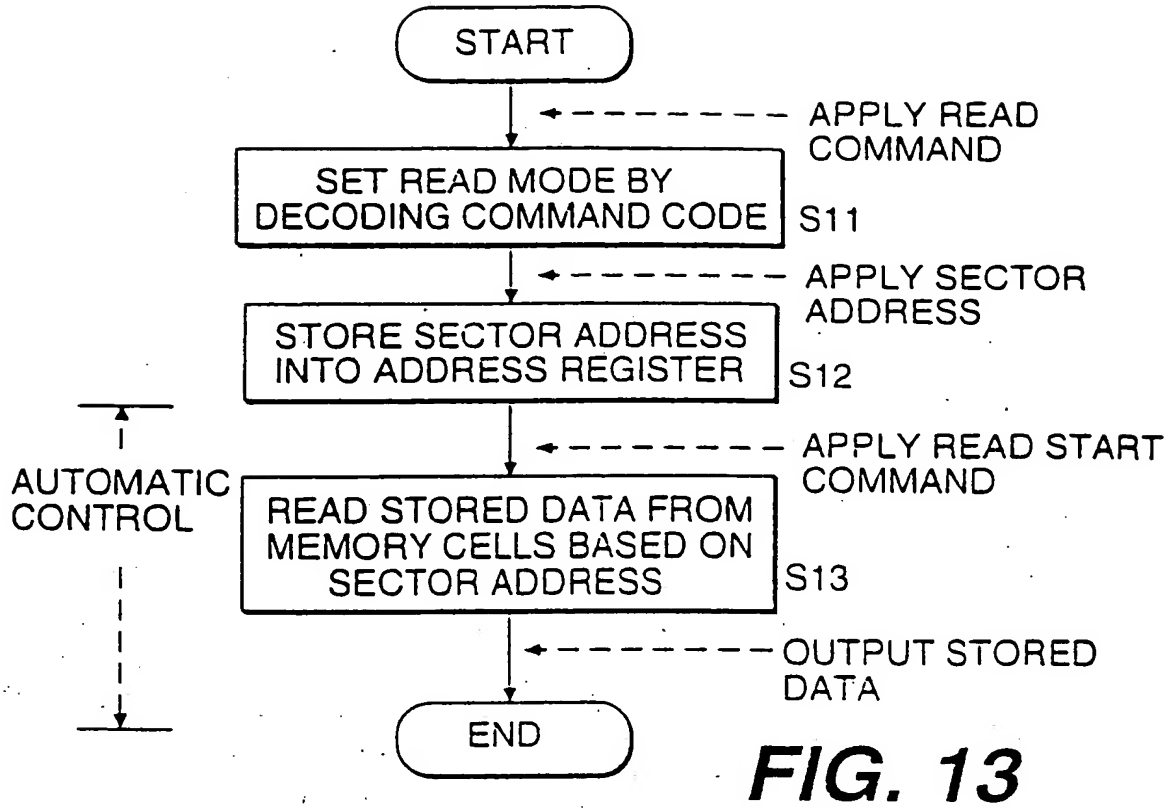

START
APPLY READ COMMAND
SET READ MODE BY DECODING COMMAND CODE
S11
APPLY SECTOR ADDRESS
STORE SECTOR ADDRESS INTO ADDRESS REGISTER
S12
AUTOMATIC CONTROL
APPLY READ START COMMAND
READ STORED DATA FROM MEMORY CELLS BASED ON SECTOR ADDRESS
S13
OUTPUT STORED DATA
END

FIG. 13

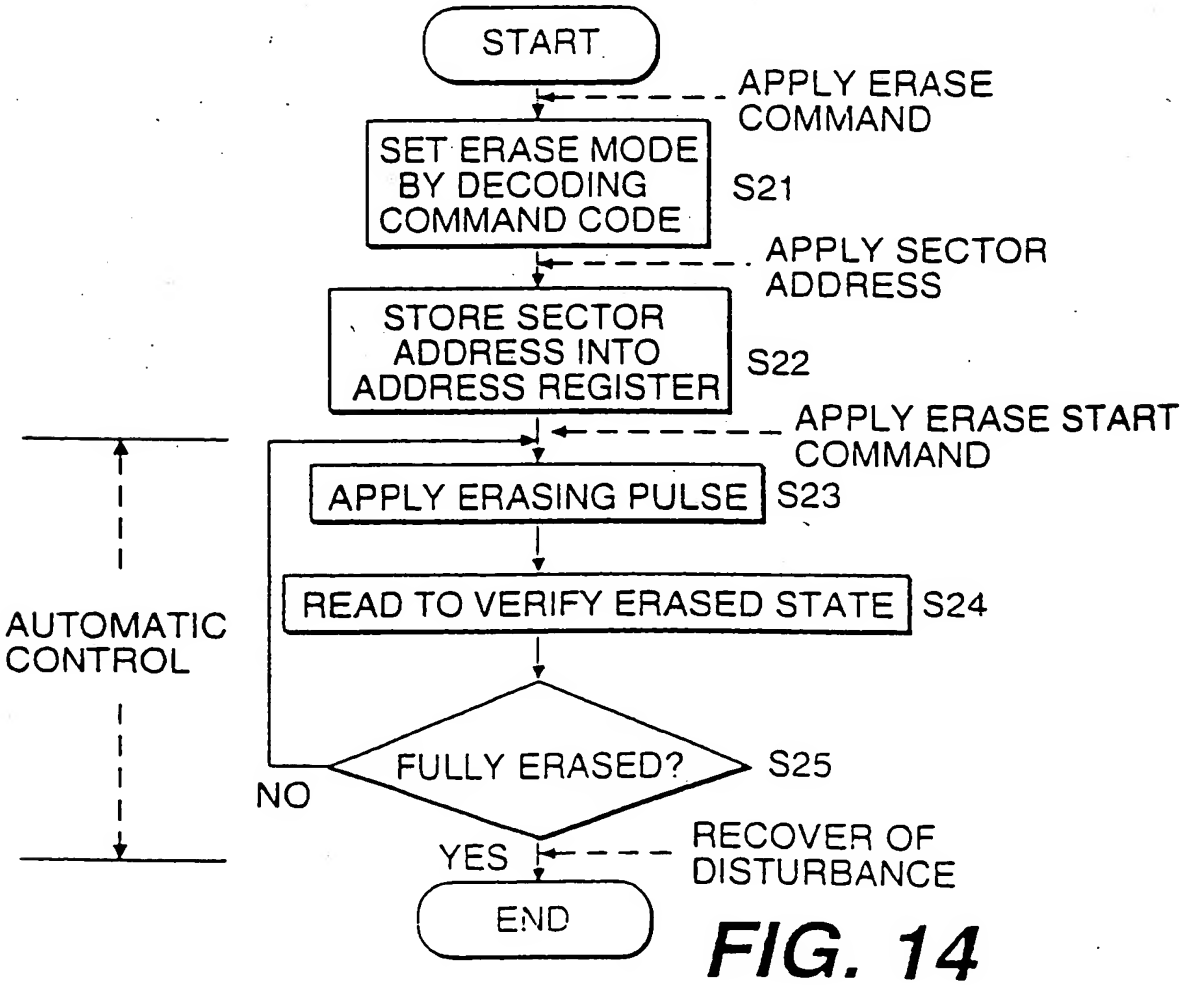

START
APPLY ERASE COMMAND
SET ERASE MODE BY DECODING COMMAND CODE
S21
APPLY SECTOR ADDRESS
STORE SECTOR ADDRESS INTO ADDRESS REGISTER
S22
APPLY ERASE START COMMAND
APPLY ERASING PULSE
S23
READ TO VERIFY ERASED STATE
S24
AUTOMATIC CONTROL
FULLY ERASED?
S25
NO
YES
RECOVER OF DISTURBANCE
END

FIG. 14

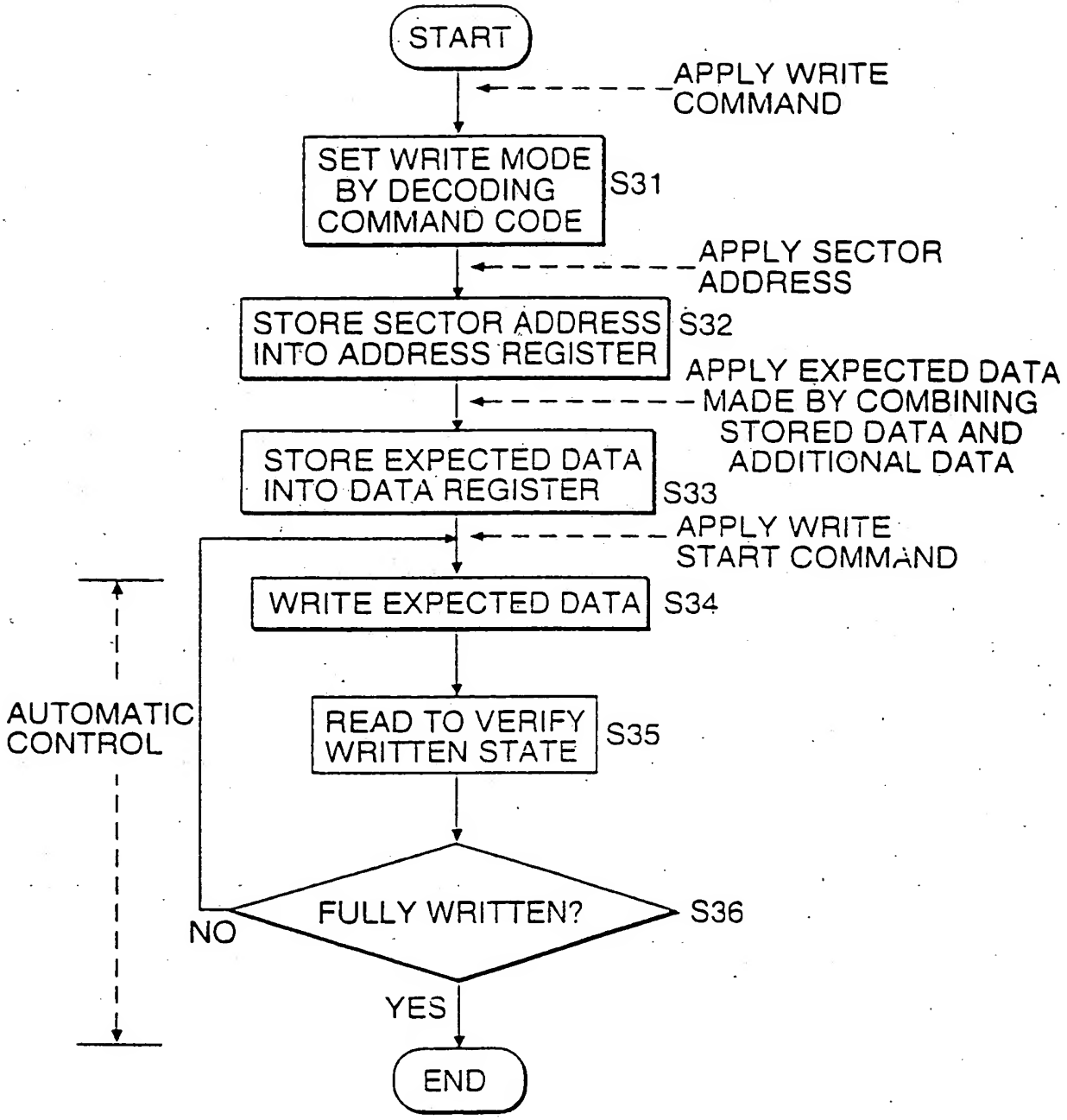

START
APPLY WRITE COMMAND
SET WRITE MODE BY DECODING COMMAND CODE
S31
APPLY SECTOR ADDRESS
STORE SECTOR ADDRESS INTO ADDRESS REGISTER
S32
APPLY EXPECTED DATA MADE BY COMBINING STORED DATA AND ADDITIONAL DATA
STORE EXPECTED DATA INTO DATA REGISTER
S33
APPLY WRITE START COMMAND
WRITE EXPECTED DATA
S34
READ TO VERIFY WRITTEN STATE
S35
FULLY WRITTEN?
S36
NO
YES
END
AUTOMATIC CONTROL

FIG. 15

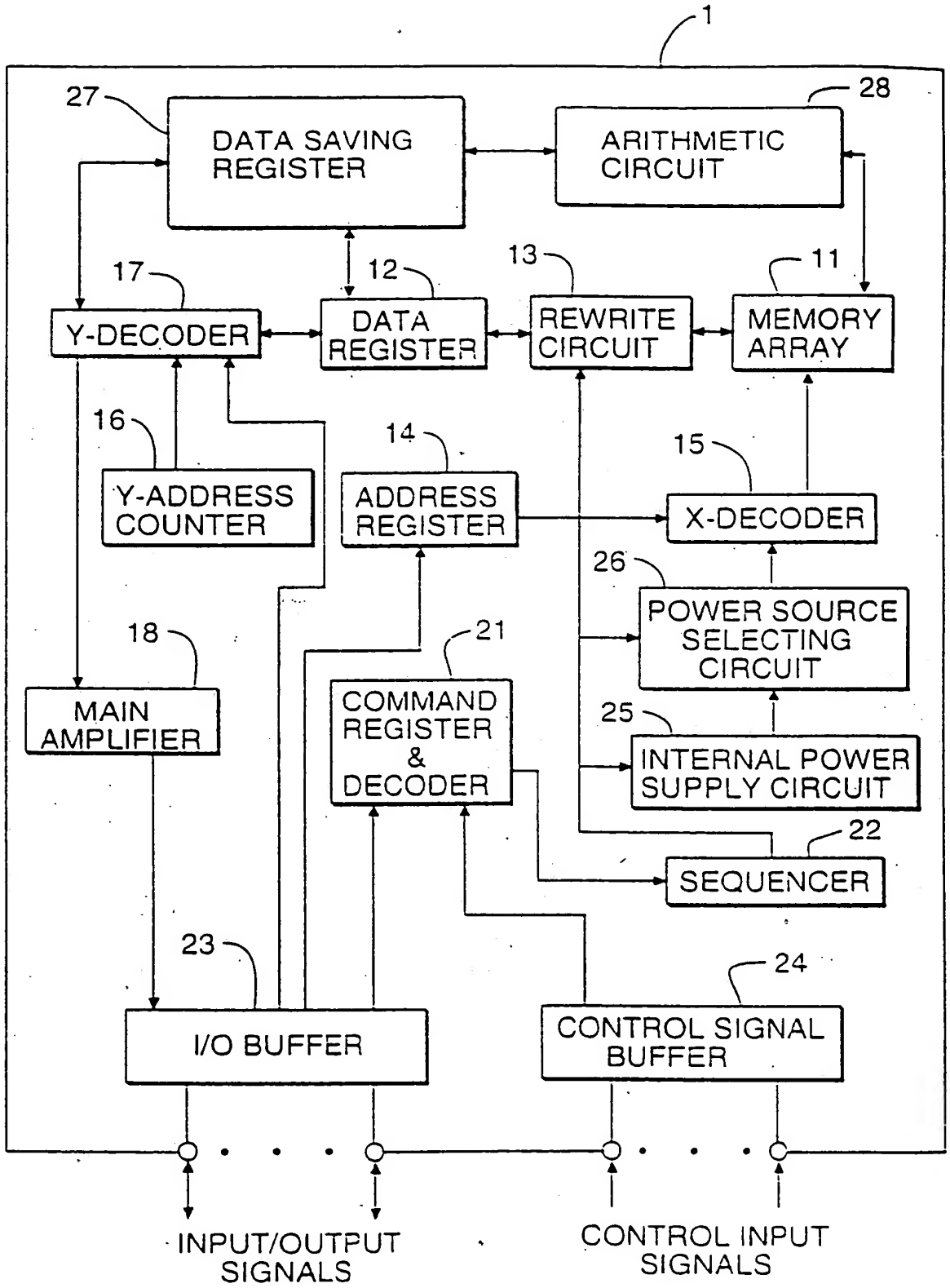

1
27
DATA SAVING REGISTER
28
ARITHMETIC CIRCUIT
17
12
13
11
Y-DECODER
DATA REGISTER
REWRITE CIRCUIT
MEMORY ARRAY
16
14
15
Y-ADDRESS COUNTER
ADDRESS REGISTER
X-DECODER
26
POWER SOURCE SELECTING CIRCUIT
18
21
MAIN AMPLIFIER
COMMAND REGISTER & DECODER
25
INTERNAL POWER SUPPLY CIRCUIT
22
SEQUENCER
23
24
I/O BUFFER
CONTROL SIGNAL BUFFER
INPUT/OUTPUT SIGNALS
CONTROL INPUT SIGNALS

FIG. 16

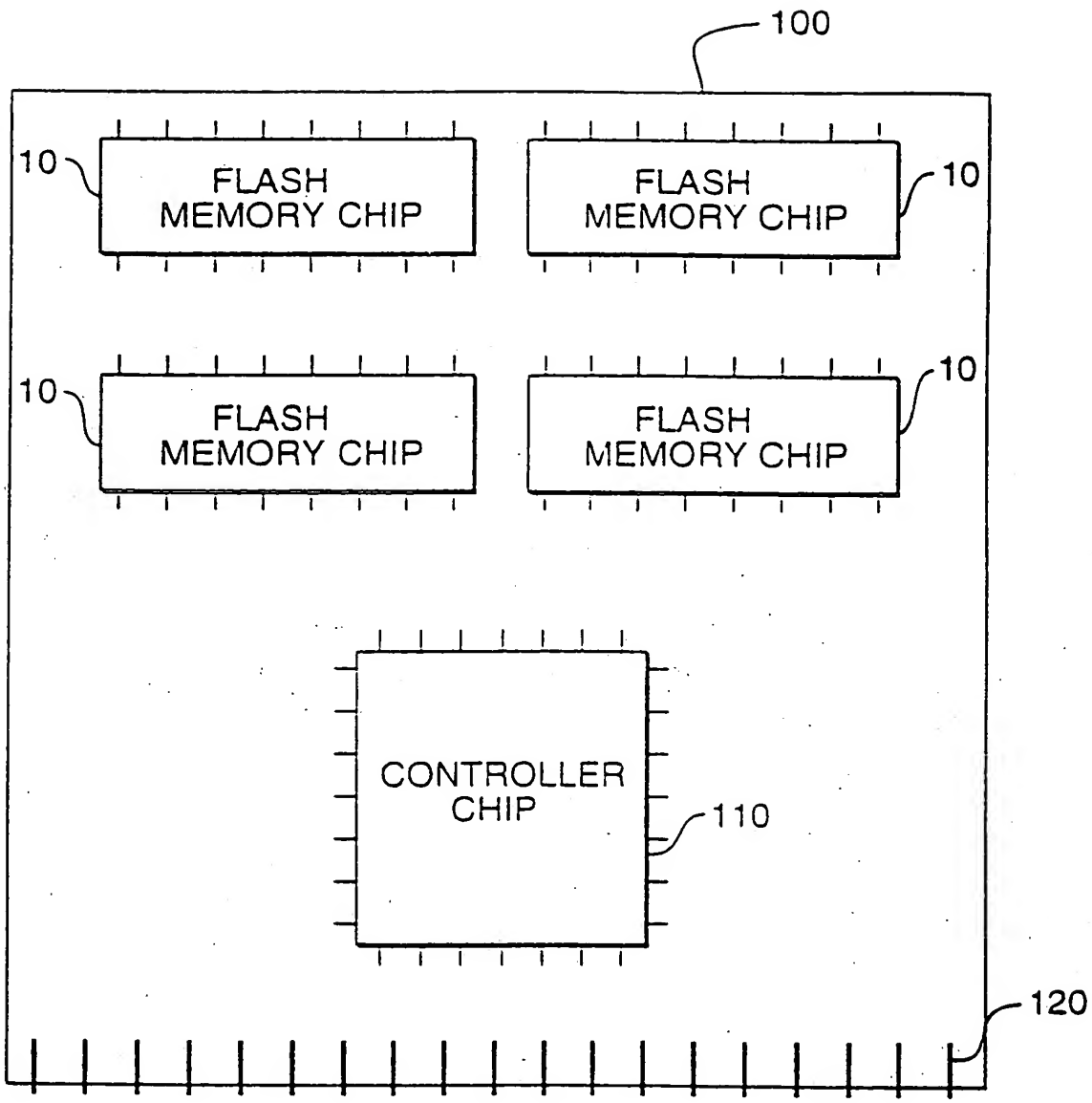

100
10
FLASH MEMORY CHIP
10
FLASH MEMORY CHIP
10
FLASH MEMORY CHIP
10
FLASH MEMORY CHIP
CONTROLLER CHIP
110
120

FIG. 17

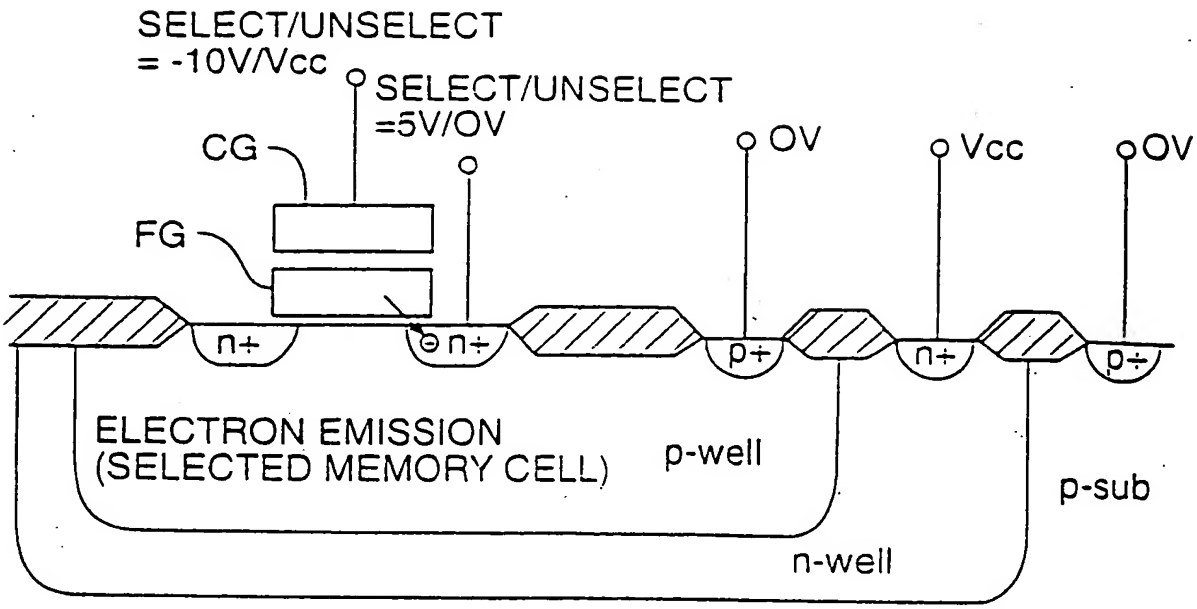

SELECT/UNSELECT
= -10V/Vcc
SELECT/UNSELECT
=5V/OV
CG
FG
OV
Vcc
OV
n+
n+
p+
n+
p+
ELECTRON EMISSION
(SELECTED MEMORY CELL)
p-well
p-sub
n-well

FIG. 18

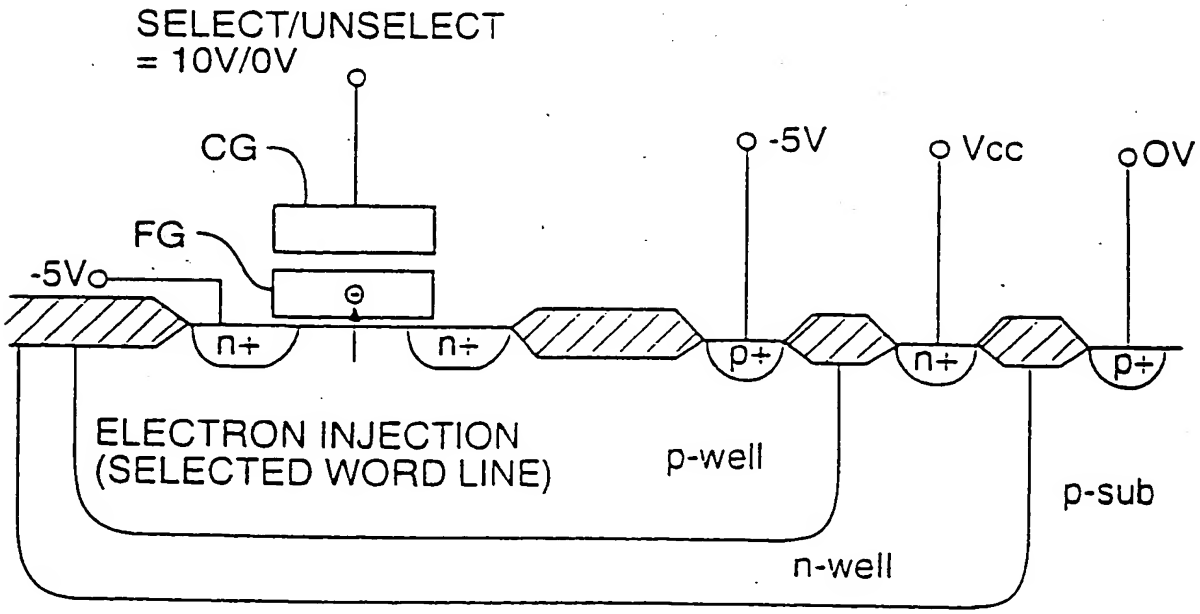

SELECT/UNSELECT
= 10V/0V
CG
FG
-5V
-5V
Vcc
OV
n+
n+
p+
n+
p+
ELECTRON INJECTION
(SELECTED WORD LINE)
p-well
p-sub
n-well

FIG. 19

PRIOR ART

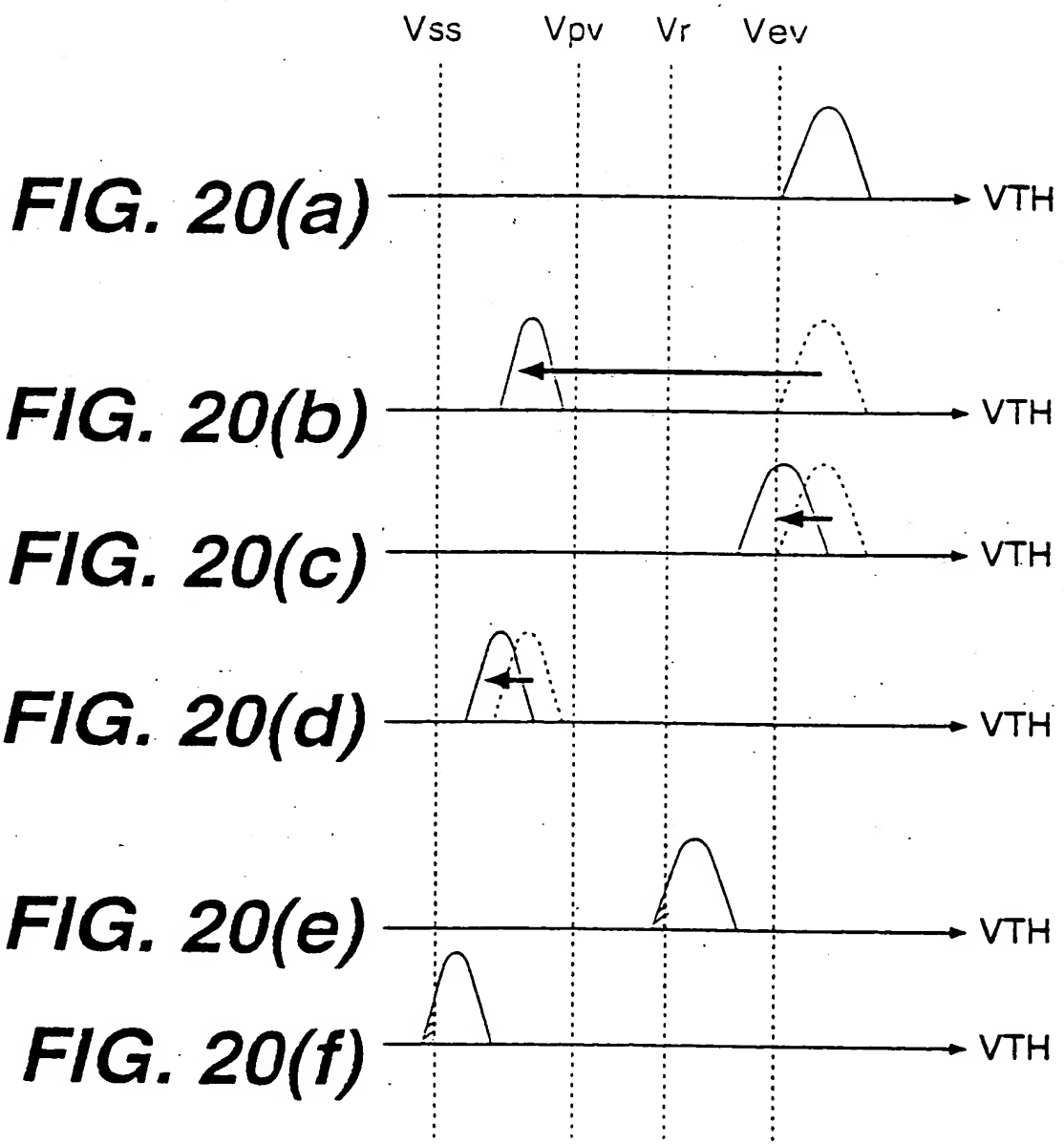


FIG. 20(a)

FIG. 20(b)

FIG. 20(c)

FIG. 20(d)

FIG. 20(e)

FIG. 20(f)

PRIOR ART

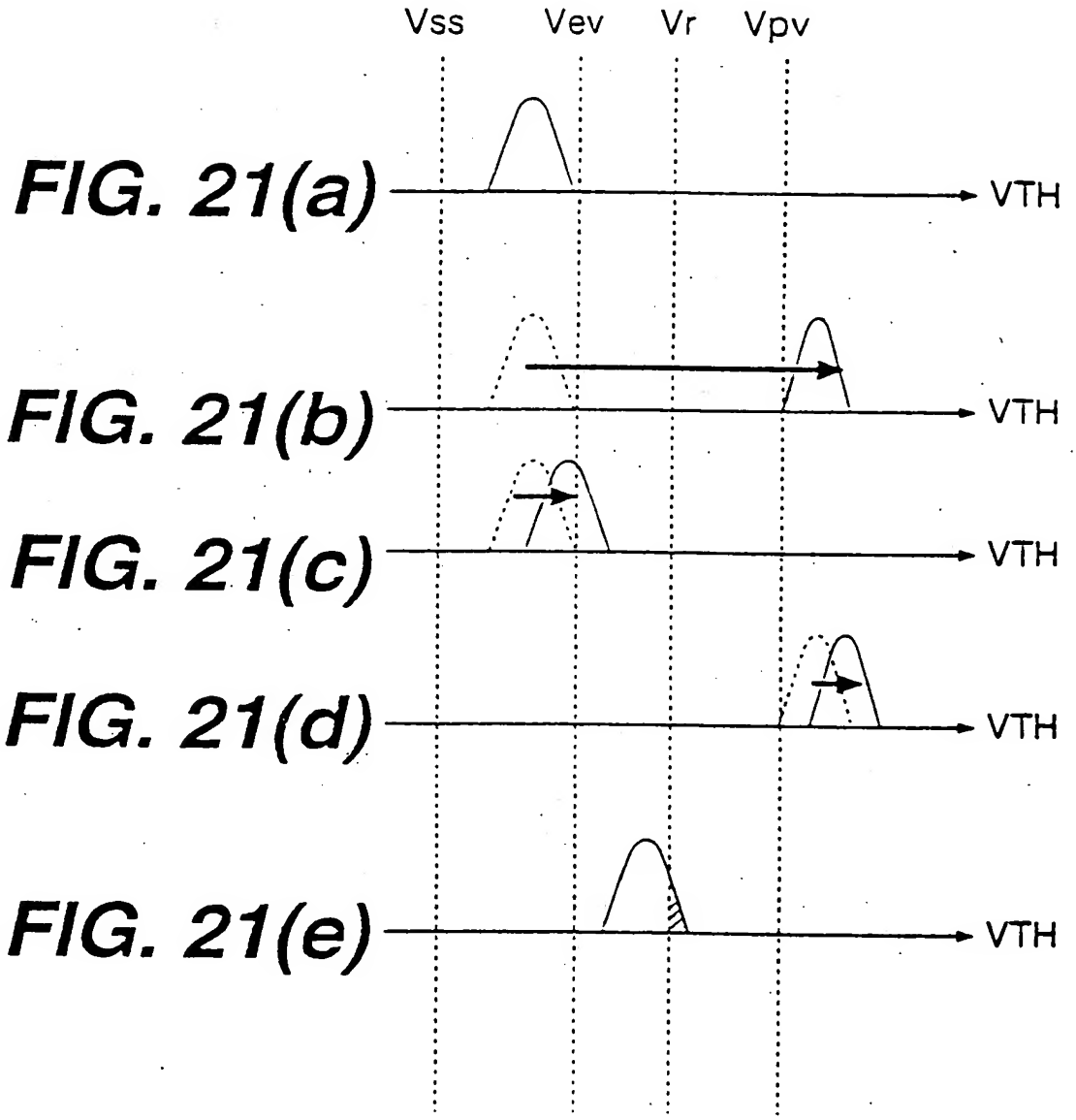


FIG. 21(a)

FIG. 21(b)

FIG. 21(c)

FIG. 21(d)

FIG. 21(e)

FIG. 22(a)

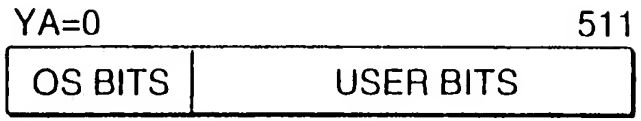
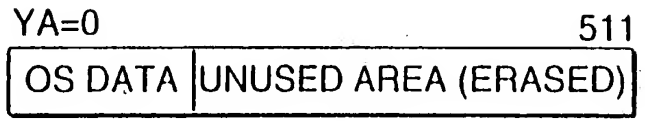


FIG. 22(b)



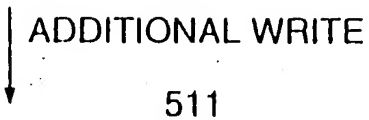


FIG. 22(c)

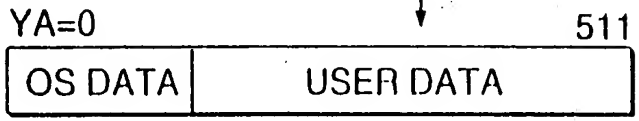


FIG. 22(d)

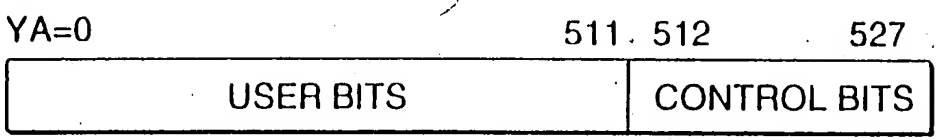
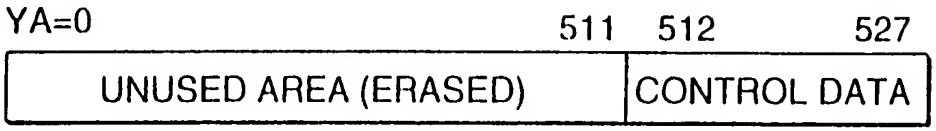


FIG. 22(e)



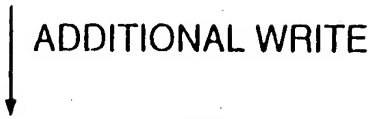
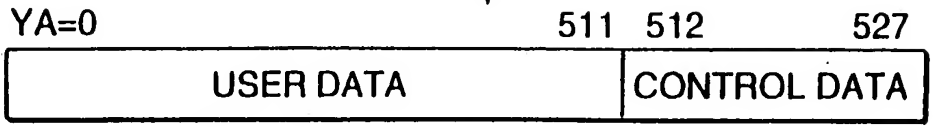


FIG. 22(f)



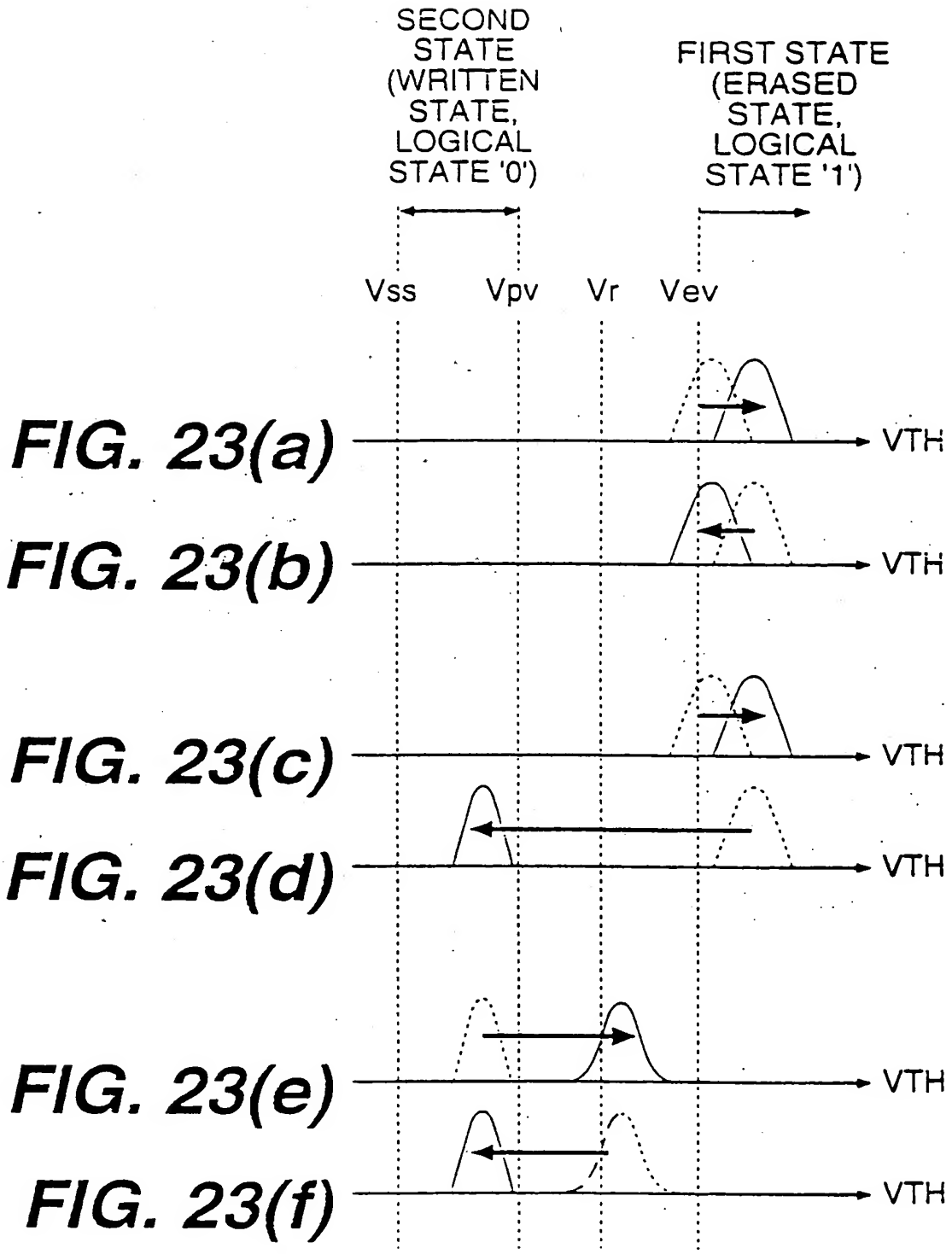


FIG. 23(a)

FIG. 23(b)

FIG. 23(c)

FIG. 23(d)

FIG. 23(e)

FIG. 23(f)

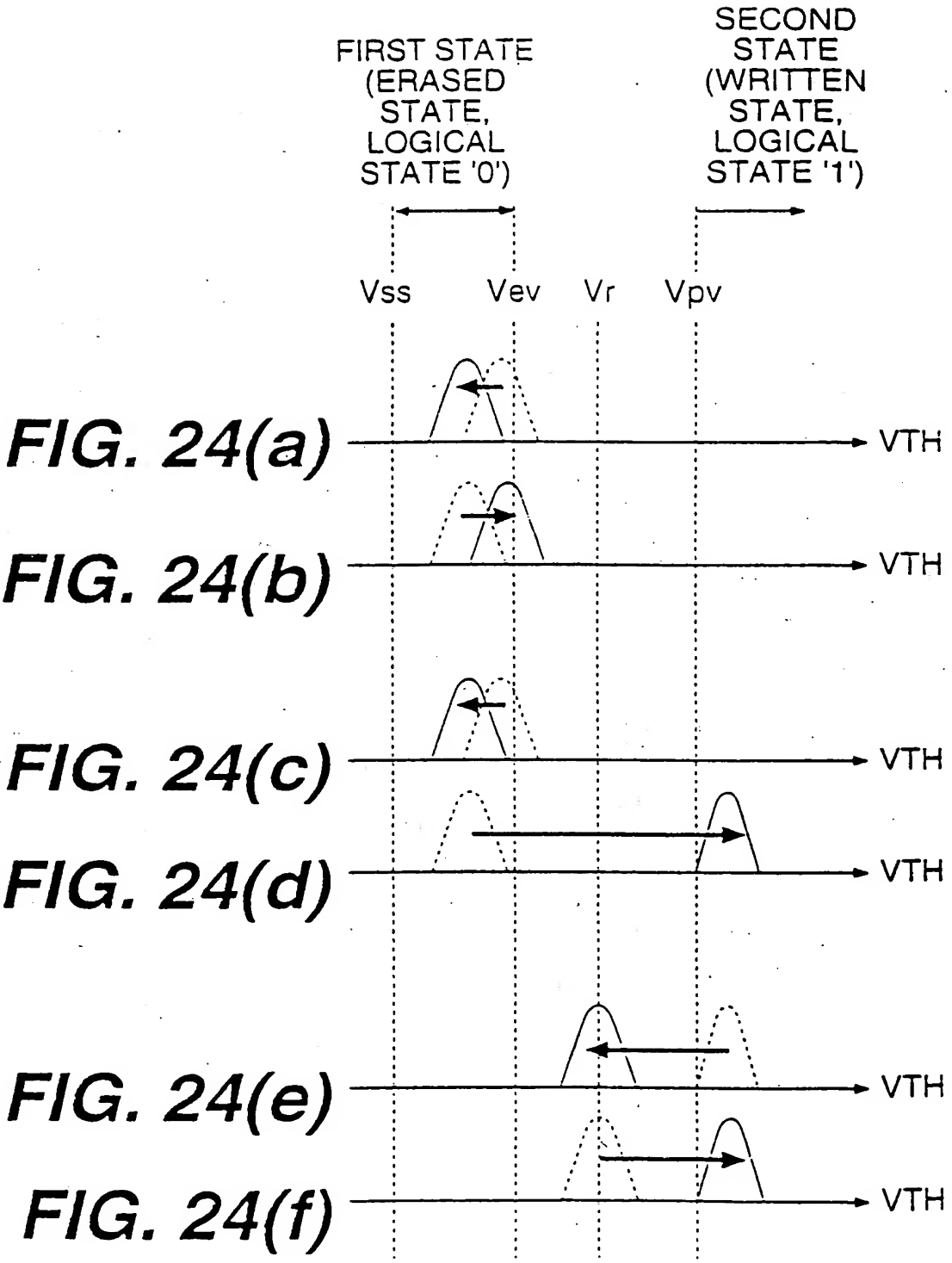


FIG. 24(a)

FIG. 24(b)

FIG. 24(c)

FIG. 24(d)

FIG. 24(e)

FIG. 24(f)